Software Implementation of 3msec Dwell Time for Beam Steering Unit of Troop Level Radar

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I Abstract:

The paper presents an implementation of 3ms dwell time for Beam Steering Unit (BSU) of Troop Level Radar (TLR). BSU is an integral part of phased array radar, which does the necessary computation and directs the beam in the desired direction electronically. Dwell Time is the time it takes to switch from one beam position to the next beam position in space. With the dwell time of 3msec, TLR would be capable of guiding 8 missiles towards 4 targets simultaneously.
Simulations were performed, actual dwell time achieved with the new software is 2.5msec.

Key Words: BSU, TLR, FLR, Dwell Time

II INTRODUCTION

Beam Steering Unit (BSU) is an integral part of phased array radar, which does the necessary computation and directs the beam in the desired direction. It is responsible for steering the beam electronically. The basic block diagram of BSU is shown in Figure 1.

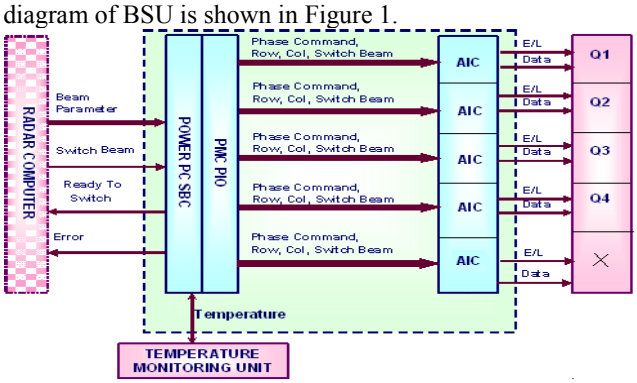

Fig 1: Block Diagram of Beam Steering Unit

The BSU is composed of two modules-

1. **Beam Steering Computer (BSC) :**
   - Processor based card
   - Receives beam parameters from RC via Ethernet link and temperature information from TMU on serial link and calculates phase commands using standard tables, collimation tables and phase command table.
   - Sends the phase command data together with PCM row and column information to the AIC in a 16 bit data format.
2. **Array Interface Card (AIC) :**
   - FPGA based card
   - Responsible for generating the output DATA and E/L (Enable/Load) signals from the phase values received from BSC for each of the PCMs
   - 4 AICs for each of the 4 quadrants of the C-Band Array and 1 AIC for 1 X-band Array

III DESIGN APPROACH

The dwell time for TLR Radar is 3ms. It is a requirement that TLR Radar must have the same hardware configuration as FLR radar. The output timings for the signals from BSU that are fed to the PCMs is fixed as per the requirements of PCMs. Therefore under the mentioned requirements, the design approach to achieve 3ms dwell time with the present hardware is:

- Reduction in the input timings
- Optimization of processes to reduce processing times
- Optimization of timings in transfer of data through interfaces

IV SOFTWARE IMPLEMENTATION OF 3msec DWELL TIME FOR BSU-TLR

The BSU software can be further divided into 2 parts:

1. Array Interface Card FPGA (VHDL) Software
2. Beam Steering Computer Application Software

As per the design approach, the software for both BSC and AIC have been implemented to achieve the dwell time of 3ms. The software implementation for both the softwares has been discussed in detail in the further sections.

V AIC SOFTWARE DESIGN FOR 3ms DWELL TIME OPERATION

The idea behind the software architecture of AIC Software for 3ms Dwell Time Operation is to reduce the time for input process. The output signals i.e. E/L and DATA signals specification and output pattern is fixed as per the specifications of PCMs and the antenna array design. So the time in output of E/L and DATA signals i.e. output process time cannot be changed. The operation time can be reduced by reducing input time and processing time to generate the output.

Fixed Parameters

i. 16-bit input from PMC-PIO card to FPGA Card
ii. One Enable O/P cycle = 32 usec, using all DATA lines. Next Enable O/P has to be atleast 32 usec+T to avoid overlapping.

So o/p side fixed parameter cannot be changed. The change has to be adapted from input side and in FPGA software architecture.

1. AIC Software Design Details

For getting the reduction in input and processing time following points have been implemented in the Software architecture for AIC for the dwell time of 3ms:

- Input data from BSC does not contain any row no. The row no. is generated internally in AIC S/W. Now the 16 bit i/p data contains 2 phase values for 2 PCMs, which means the input time for receiving data for a single

column is reduced to half. This subsequently reduces the total data input time to half.

- Data for each column is stored in individual RAMs (each column data has individual RAM assigned to it) as shown in Figure 2. This makes the input speed independent of the output, thereby increasing the input data rate.
- Using the column no. and the phase values stored in individual RAMs, output signals DATA and E/L for each of the PCMs is generated with both E/L and DATA generator blocks working synchronously and then sent serially to the PCMs.

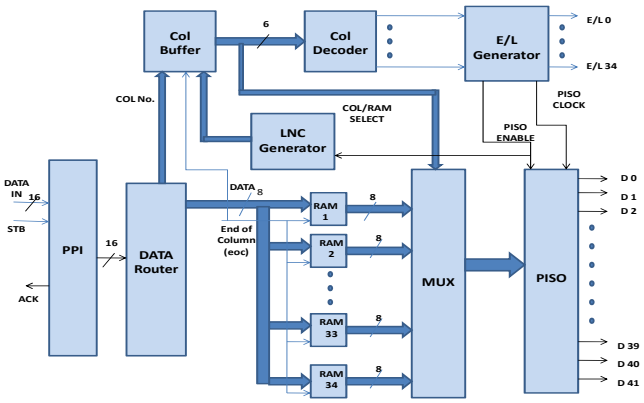

Figure 2: Software Architecture Block Diagram for AIC Software

2. AIC Software Implementation and Software Functioning

The AIC generates DATA and E/L signals using the 16 bit data received from the TPMC Card that is actually coming from SBC.

The AIC Software functioning is as follows:

- BSC sends 16 bit data (1word) along with strobe which is an active low signal through PMC-PIO Card, which is received by the PPI module of AIC Software.
- The message IDs are sent in a sequence from BSC: RESET, Enable, Maximum Row no. and Column No. data. Thereafter column no. and phase data is sent for all PCMs. This sequence is shown in Figure 3.

The Sequence of messages between BSC and AIC is:

- RESET
- ENABLE
- Array Dimension Message containing the maximum row and column no.
- Col No. 0
- Phase Command Data 1, Phase Command Data 0
- Phase Command Data 3, Phase Command Data 2
- .....
- Phase Command Data (Max. Row No./2), Phase Command Data 0 ((Max. Row No./2)-1)
- End of Row Message
- Col No. 1
- Phase Command Data 1, Phase Command Data 0
- Phase Command Data 1, Phase Command Data 0
- .....
- Phase Command Data (Max. Row No./2), Phase Command Data 0 ((Max. Row No./2)-1)
- End of Row Message
- .....
- .....
- .....
- Col No. (Max. Col. No.)
- Phase Command Data 1, Phase Command Data 0
- Phase Command Data 1, Phase Command Data 0
- .....
- Phase Command Data (Max. Row No./2), Phase Command Data 0 ((Max. Row No./2)-1)
- End of Row Message
- Switch Beam
- RESET2

Figure 3: Sequence of Messages between BSC and AIC

- Data router reads the data and sends an ACK to BSC saying that data is read and next data can be sent. After reading the data, Data Router verifies it. Depending on message ID, it will route the data to either column decoder or to the latches.
- After RESET and ENABLE, Column no. is received that is sent to column decoder which activates one of the E/L lines.
- Column no. is followed by the phase command data for all rows of that column. The Row No. is generated internally for storing the phase command data in consequent memory locations in the RAM, using a counter that is reinitialized to 0 when the next col no. comes. Before the next col no. data, an End of Row (EOR) data is sent to generate the End of Column (EOC) signal.
- Similarly for each column no., E/L is generated. DATA outputs are generated for each of the E/L signal.
- After all column data has been sent, a Switch Beam command is sent. After the Switch Beam command, a reset signal RESET2 is also sent that resets all the variables and reinitializes all modules.
- Data for one column is stored in a RAM eg. Data for Column 0 is stored in RAM 1, data for Column 1 is stored in RAM 2 and so on. An internal counter generates the row no. to store the data for each subsequent row correctly in the RAM. The EOC signal is used for selecting the RAM in which the data must be stored.
- The data input is faster than the data output, so each block of data for a particular column is stored subsequently in each of the RAMs. When one E/L and DATA output is complete a signal is generated to increase the counter value to generate the output for the next column. Hence data for a particular column is available beforehand but is output only when the previous output has finished.
- Column Buffer stores the col no. data and on receiving the LNC signal (that increases from 0 to 34), the next col no. is selected and output to the column decoder to generate E/L signal for that col no. This 6 bit Col output is input on the select lines of the MUX that selects the RAM for that col no.
- The parallel data from MUX goes to PISO that is converted to serial data using the PISO generator.
- E/L generator and PISO work synchronously. The clock and enable for the PISO is generated by the E/L Generator. So E/L and DATA are available simultaneously for the PCMs.

3. Simulation Results For AIC 3ms Software

The BSU TLR AIC software for 3msec Operation was simulated using Xilinx ISE Simulator tool. Figure 4 shows the Simulation results of the FPGA software. All the timings of output E/L and DATA signals were verified and found to be OK. All internal signals were verified and the software modules were checked for proper implementation.

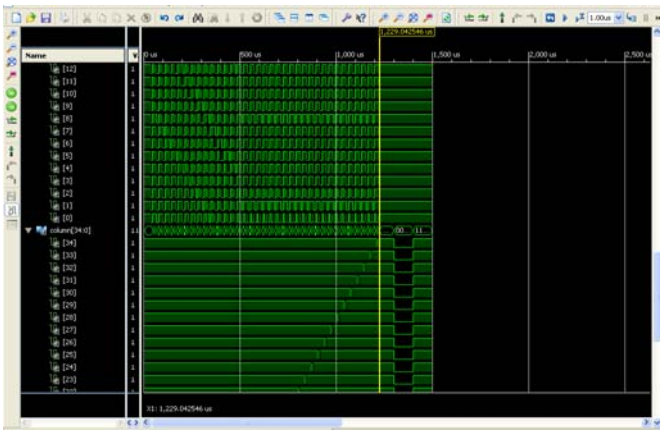

Fig4: Simulation results for AIC Software for 3ms Dwell Time operation

VI BSC APPLICATION SOFTWARE DESIGN FOR 3ms DWELL TIME OPERATION

BSU receives the beam parameters (alpha, beta, C-Band & X-Band frequency) from the Radar Controller on an Ethernet interface. It also obtains the temperature information from the TMU. These are used for calculations of phase gradients. The BSC then calculates the phase values using the phase gradient, standard tables, command table and collimation tables files.

1. BSC Software Design and Implementation of BSC Application Software

The data flow diagram for calculation of phase values is shown in the Figure 5.

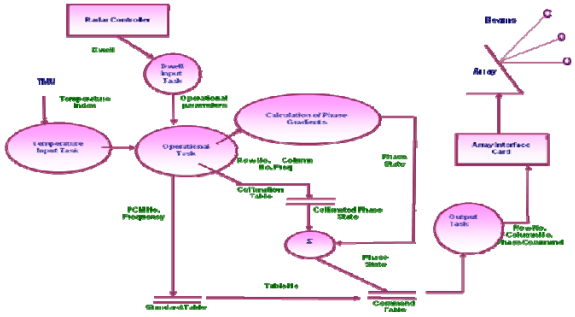

Figure 5: BSU Phase Value Calculation Data Flow Diagram

- After calculating the phase commands, BSC gives the phase values together with the PCM locations as column number, values in the eight bit parallel form to the AICs that further generate the E/L and Data Signals to be given to the PCMs.
- The data is sent through the ports of PMC PIO (PMC Parallel I/O) Card to the AICs. Every time a data is transferred from BSC to PIO Card, driver for the PIO card is called.
- Hence in the new software architecture instead of sending one by one data for every PCM, all the phase values are calculated and stored in an array and sent as a single block to the AIC. Using this method, the PMC-PIO Card driver is called only once thereby reducing the time required for sending phase values from BSC to AIC.
- Also the Buffer size for PMC-PIO Card port is reduced for the software for 3ms. This is because now only half of the words would be required for sending phase command data, as now one word contains phase commands for 2 rows.
- The flowchart for BSC Application Software for dwell time of 3ms is shown in Figure 6.

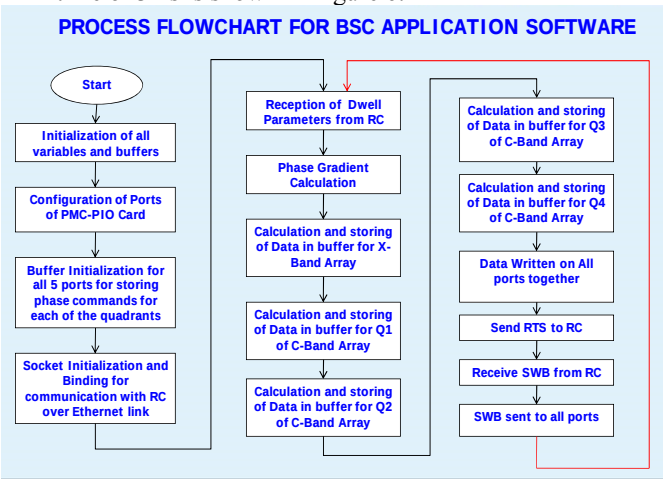

Figure 6: Flowchart of BSC Application Software

VII VALIDATION RESULTS

1. Validation Results through Fixed Data Software

Testing of BSU 3ms Software performed using Fixed Data Software to check the BSU operation for correct outputs. All outputs were found OK. Comparison of Timings achieved for Individual Functions of BSU Application Software for BLR-III & TLR is as shown in Table 1.

Table 1: Comparison of Timings of Functions in Application Software for BLR-III and TLR BSU

BSC Application Software individual Function	For 5ms Dwell Time, Function Timing	For 3ms Dwell Time, Function Timing	REMARKS
PaPb (us)	79	8	Saving of 1msec in optimisation of device drivers and other optimisations
X (us)	210	125	
Q1 (us)	358	136	
Q2 (us)	337	140	
Q3 (us)	354	139	
Q4 (us)	354	134	
Sending Data to all Ports (us)	1414	816	Improvement of 600 usec with optimisation of data transfer as per new S/W architecture
RTS Sending (us)	124	15	Improvement of 600 usec with optimisation of data transfer as per new S/W architecture
SWB reception (us)	133	20	
SWB sent to all Ports (us)	1157	821	
Total Time (us)	4799	2354	Time difference of 2445 usec(2.4 msec)

2. Validation Results by Measuring the Dwell Timing on CRO

Figure 7 shows the Timing Measurement between one LOAD pulse to other showing the Dwell Time obtained from BSU 3ms Software. The Load-to-Load time is measured as = ΔX = 2.42ms.

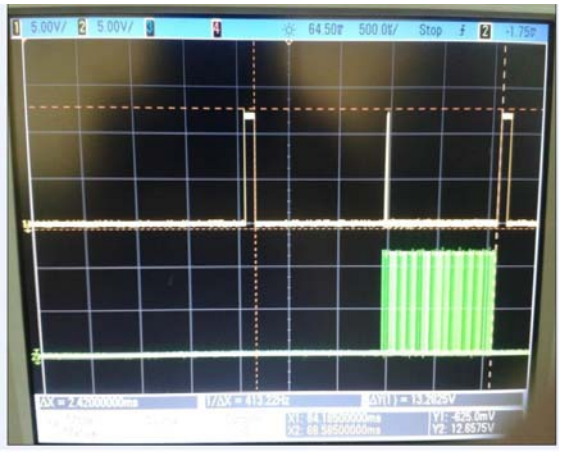

Figure 7: Timing Measurement between one LOAD pulse to other showing the Dwell Time using BSU 3ms Software. Load-to-Load time measured= ΔX = 2.42ms

3. NFTR Results for BSU TLR 2.5ms Operation

Collimation was performed at NFTR using the BSU 3ms software. Results were found to be OK with respect to specifications as shown in Figure 8. The results for steering from BSU at 2.5ms dwell time were obtained in NFTR for both C-Band and X-Band antennas, as shown in Figure 9 and Table2.

Table 2: Final Results of Steering for TLR C-BAND & X-BAND Antenna

SLL: Sidelobe level

Freq GHz (C-BAND Array Results)	Commanded Angle (Az , El) deg	Peak Sidelobe (dB)			
		Azimuth		Elevation	
		SLL Actual (Specs) (dB)	Beam width Actual (specs) (deg)	SLL Actual (Specs) (dB)	Beam width Actual (specs) (deg)
5.58 Collimation	**0,0**	**-28.47** (≤-26)	**1.69** (1.7 ± 0.2)	**29.64** (≤-25)	**1.75** (1.7 ± 0.2)
5.58 (2.5msec Steering)	**0,0**	**-29.03** (≤-26)	**1.74** (1.7 ± 0.2)	**28.50** (≤-25)	**1.76** (1.7 ± 0.2)
5.40 (2.5msec steering)	**30,30**	**-28.24** (≤-22)		**26.49** (≤-21)	
Freq GHz (X-BAND Array Results)	**Commanded Angle (Az , El) deg**	**Peak Sidelobe (dB)**			
		Azimuth(SLL)		**Elevation(SLL)**	
		Actual (Specs) dB		**Actual (Specs) dB**	
9.32 (2.5msec Steering)	**30,30**	**-22.09** (≤-20)		**29.09** (≤-22)	

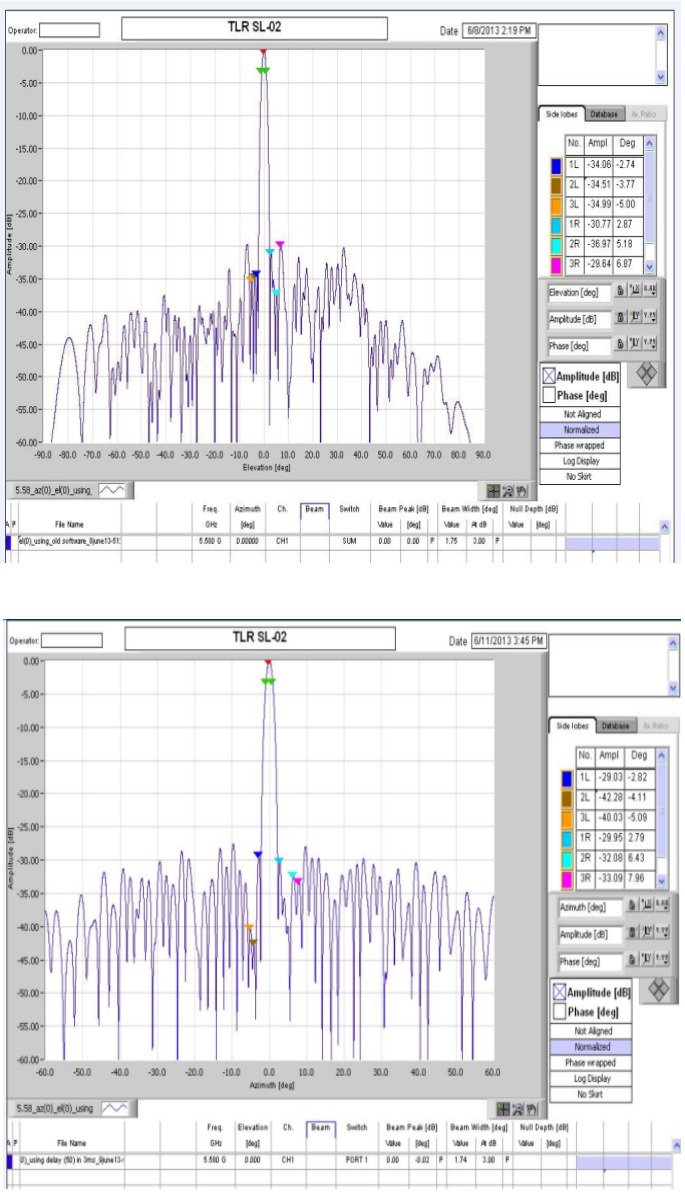

Figure 8: Cartesian Plot in Azimuth Elevation at Azimuth=0, Elevation=0, Freq=5.58GHz during Collimation at NFTR

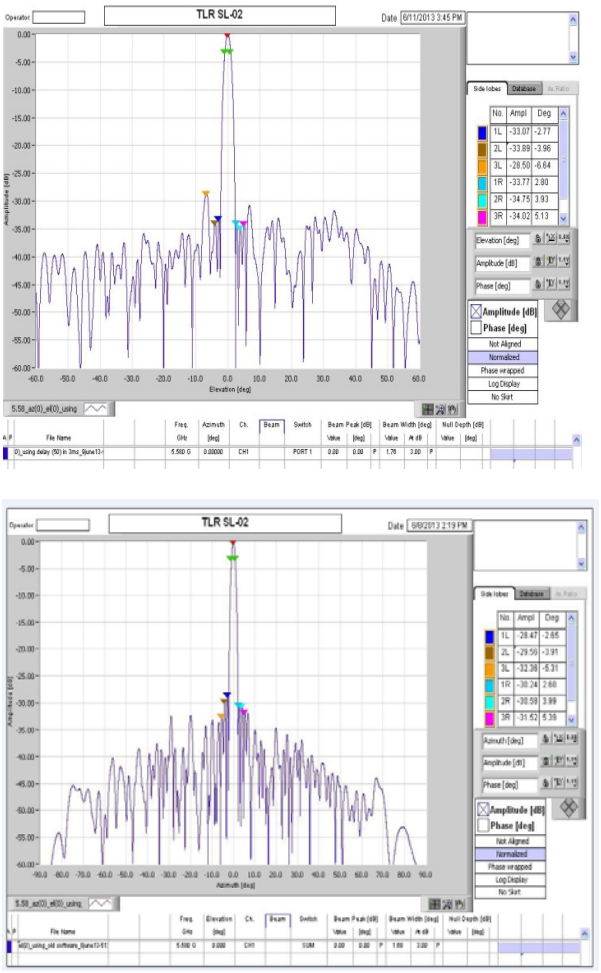

Figure 9: Cartesian Plot in Azimuth Elevation at Azimuth=0, Elevation=0, Freq=5.58GHz using 2.5msec Steering Software at NFTR

VIII APPLICATION OF TECHNOLOGY MODULE IN MAIN PRODUCT/SYSTEM

TLR antenna is a phased array & beam is electronically steered using BSU. For achieving the desired surveillance of 10 targets, tracking of 10 targets & guidance of 8 missiles towards 4 targets simultaneously, beam steering less than 3msec was one of the main requirements in antenna system. Beam steering of 2.5msecs achieved with the new software architecture and the same hardware as used in FLR. BSU Software controls both C-Band & X-band array simultaneously for tracking with C-band & missile guidance with X-Band antenna. BSU with 2.5msec dwell time gives 400 beam positions/sec to perform the desired radar functions of target capability as (also derive advantages of waveform agility) required in TLR.

CONCLUSION

The design for 3msec dwell time for BSU-TLR using the same hardware as used in the FLR has been successfully implemented and validated. As shown in the simulation and validation results, the actual dwell time achieved with the new software is 2.5msec for BSU.

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BIO DATA OF AUTHORS

Vinay Kumar Sawnani has completed B.E.(Electronics) from Nagpur University, M.Tech(Digital Signal Processing) from NSIT,Delhi in 2000. He started his career in embedded control systems working in design of microcontrollers & signal processing systems. Currently he his working as a Manager in D&E-Antenna, Bharat Electronics Limited, Ghaziabad. He is heading the Embedded Control Systems group in D&E-antenna and has worked on projects like FLR, WLR, TLR,TCR, Rohini etc. with LRDE.

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